WHAT IS CLAIMED IS:

1   1.   A voltage regulation system for multiword programming in a non volatile

2   memory, for example of the Flash type, with low circuit area occupation, wherein the memory

3   comprises at least a memory cell matrix organized in cell rows and columns and with

4   corresponding circuits responsible for addressing, decoding, reading, writing and erasing the

5   memory cell content, each cell having a drain terminal connected to a matrix column and biased

6   in the programming step with a predetermined voltage value by a program load circuit associated

7   with each matrix column, the system further including, in parallel with each program load

8   circuit, a conduction-to-ground path enabled by a controlled active element.

1   2.   The system according to claim 1, wherein the controlled active element is a pass

2   transistor receiving on the control terminal thereof a first enabling signal.

1   3.   The system according to claim 2, wherein the first enabling signal is

2   complementary to a second enabling signal applied to the corresponding program load circuit.

1   4.   The system according to claim 1, wherein the conduction-to-ground path is a

2   redundant current path.

1   5.   The system according to claim 1, wherein the conduction-to-ground path is a

2   dummy current path.

1   6.   A non-volatile memory circuit, comprising:

2   a non-volatile memory cell coupled to a bit line and a word line; and

3   a selectively actuated conduction to ground path coupled to the bit line.

1   7.   The circuit of claim 6 wherein the non-volatile memory cell comprises a floating

2   gate transistor having its drain terminal connected to the bit line and its gate connected to the

3   word line.

1   8.   The circuit of claim 6 further including a bit line biasing circuit coupled to the bit

2   line, the selectively actuated conduction to ground path being connected in parallel with the bit

3   line biasing circuit.

1   9.   The circuit of claim 6 wherein the selectively actuated conduction to ground path

2   is coupled to the bit line through at least a column decoding circuit.

1   10.   The circuit of claim 6 wherein the selectively actuated conduction to ground path

2   is coupled to the bit line through at least a bit line biasing circuit.

1   11.   The circuit of claim 10 wherein the bit line biasing circuit and the selectively

2   actuated conduction to ground path are oppositely activated.

1   12. A non-volatile memory, comprising:

2   a memory matrix including a plurality of memory cells arranged in columns, each

3 associated with a bit line, and rows, each associated with a word line;

4   a column programming circuit coupled between a programming voltage source

5 and each bit line and activated in response to a first control signal; and

6   a bypass path circuit for each bit line and coupled between the programming

7 voltage source and ground and activated in response to a second control signal.

1   13. The memory of claim 12 wherein each memory cell comprises a floating gate

2 transistor having its drain terminal connected to the bit line and its gate connected to the word

3 line.

1   14. The memory of claim 12 wherein, for each column, the first and second control

2 signals are complementary.

1   15. The memory of claim 12 further including a column decoding circuit for each

2 column.

1   16. The memory of claim 12 wherein the bypass path circuit comprises a pass

2 transistor for each column coupled between the programming voltage source and ground.

1   17.   A voltage regulation system for a non volatile memory including a memory cell

2   matrix organized in cell rows and columns, comprising:

3   a program load circuit for each matrix column that biases each memory cell in a

4   selected matrix column with a predetermined voltage value during a programming operation; and

5   a conduction-to-ground path for each matrix column, each path being enabled

6   when its associated matrix column is not selected during the programming operation.

1   18.   The system of claim 17 wherein each memory cell comprises a floating gate

2   transistor having its drain terminal connected to a bit line for a column and its gate connected to

3   a word line for a row.

1   19.   The system of claim 17 further including a column decoding circuit for each

2   column.

1   20.   The system according to claim 17, wherein the conduction to ground path

2   includes a controlled active element comprising a pass transistor receiving on a control terminal

3   thereof a first enabling signal.

1   21.   The system according to claim 20, wherein the first enabling signal is

2   complementary to a second enabling signal applied to the corresponding program load circuit.

1   22.   The system according to claim 17, wherein the conduction-to-ground path is a

2   redundant current path for the program load circuit.

15

1   23.   The system according to claim 17, wherein the conduction-to-ground path is a

2   dummy current path for the program load circuit.